Solution

Q1

Micro-controller (embedded processor), features:

- All interface on a chip
- Less computing power
- Low cost and high volume applications

Digital Signal Processor (DSP), features:

- Highly parallel architecture for signal processing
- Include multiplier and barrel shifter hardware
- May include high speed interface for parallel processing

Q2

Find the inverse sequence for the following function:

$$F(z) = \frac{z^2 + z}{z^2 - 3z + 4}$$

Multiplication by z^{-2} in numerator and denominator gives

$$F(z) = \frac{1 + z^{-1}}{1 - 3z^{-1} + 4z^{-2}}$$

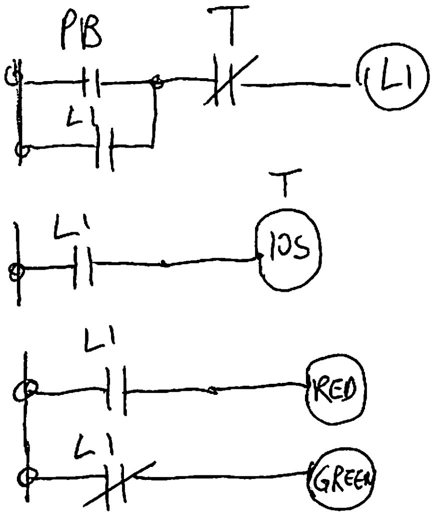
Now carry out formal long division to yield

$$\begin{array}{r|l}
 & 1 + 4z^{-1} + 8z^{-2} \\
\hline
1 - 3z^{-1} + 4z^{-2} & 1 + z^{-1} \\
 & \underline{1 - 3z^{-1} + 4z^{-2}} \\
 & \quad 4z^{-1} - 4z^{-2} \\
 & \quad \underline{4z^{-1} - 12z^{-2} + 16z^{-3}} \\
 & \qquad\qquad 8z^{-2} - 16z^{-3} \\
 & \qquad\qquad \underline{8z^{-2} - 24z^{-3} + 32z^{-4}} \\
 & \qquad\qquad\qquad\quad 8z^{-3} - 32z^{-4} \\
 & \qquad\qquad\qquad\quad \vdots
\end{array}$$

Now upon examination of the coefficients of the infinite series answer, the sequence is

$$f(0) = 1$$
$$f(1) = 4$$
$$f(2) = 8$$

Q3



← once pressed, lock on

← reset after 10 sec

← lock on ⇒ RED

← reset ⇒ GREEN

Q4

$$H(z) = \frac{\sum_{n=0}^{M} b(n)z^{-n}}{1 + \sum_{n=1}^{N} a(n)z^{-n}}$$

$$= H_1(z)H_2(z) = \left[\frac{1}{1 + \sum_{n=1}^{N} a(n)z^{-n}}\right]\left[\sum_{n=0}^{M} b(n)z^{-n}\right]$$

H2(z)= $b_0 + b(1)z^{-1} + b(2)z^{-2} + b(3)z^{-3}$

$$H_1(z) = \frac{1}{1 + a(1)z^{-1} + a(2)z^{-2} + a(3)z^{-3}}$$