[9] A.G. Phadke and J.S. Thorp, "Computer Relaying for Power System", Research Studies Press Ltd., Somerset, England, 1988.

[10] M.S. Sachdev and D.L. Waikar, "Design of the Software for a High Speed Digital Distance Relay", Proceedings of the International Conference on Power System Protection, Singapore, Sept. 1989, pp. 262-279.

## 6. ACKNOWLEDGEMENTS

The author wishes to express his sincere thanks to Dr. Philip Chin, Head of the Department of Electrical Engineering, Singapore Polytechnic, Singapore, for his encouragement during the preparation of this manuscript and for nominating him to present this paper at the conference. The author is thankful to Prof. M.S. Sachdev, Head of Dept. of Electrical Engineering, University of Saskatchewan, Canada, for introducing him to the digital relaying subject, guidance and encouragement.





# A Modified Finite Transform Algorithm for Digital Distance Protection

K. K. Li, C. Cheung
Hong Kong Polytechnic
Kowloon, Hong Kong

Y. Q. Xia
Tianjin University
Tianjin, China

Abstract: This paper presents a modified finite transform algorithm for an ultra-high-speed digital distance protection. The algorithm employs a very short data window together with a high sampling frequency. Result of simulation shows that stable operation and high operating speed are achieved even in the presence of high frequency components caused by reflected travelling waves in the transmission line. Real time simulation verifies that the technology can be implemented in low cost microprocessors.

## 1. Introduction

Digital protective relay in power system has been developing for more than twenty years[1]. Because of its advantages in characteristic-: accuracy, flexibility, user friendliness, easy testing and self-monitoring[2], the stage of commercial use has begun in recent years.

Stimulated by a need for ultra-high-speed fault clearance[3] and the availability of the appropriately priced signal processing technology, there has been growing effort on high speed digital transmission line protection[4]-[8].

During fault conditions, the voltage and current waveforms are usually distorted and consist of numerous harmonics and reflected travelling wave components [9]. However, they contain the basic information about the fault. System impedance calculation for distance relaying can be obtained by extracting the fundamental components. In general, the algorithm used should possess short data window and high sampling frequency for ultra-high-speed relay application. Short data window will introduce errors due to D.C. components, subharmonics and superharmonics. High sample frequency can reduce errors, but in the other hand it also reduces the available time for computation and a high speed microprocessor is required.

This paper presents a modified finite transform algorithm which can reduced on-line calculation and possesses high filtering function. Result of simulation shows that the calculated impedance converges rapidly. Real time simulation further proves that the algorithm can be implemented by using commonly available 16-bit microprocessor to achieve ultra fast operating speed.

## 2. Principle of the algorithm

The following transmission line equation is used as the basis of calculation:--

$$V_r(t) - R\, i_r(t) + L\, di_r(t) / dt \qquad (1)$$

Although the system voltages and currents do not conform exactly to equation (1), it is a close approximation based on the Positive Phase Sequence series inductance and resistance of the line at power frequency provided high frequency components caused by fault induced travelling waves are prefiltered [5].

Eqn.(1) has been solved by other authors in different way, but this paper presents a new approach.

The finite transform of voltage and current is given by eqn.(2) and (3) respectively,

$$\overline{V}_r(j\omega_e, t) = \int_{t-T_w}^{t} v_r(\tau)\exp(-j\omega_e\tau)\,d\tau \tag{2}$$

$$\overline{I}_r(j\omega_e, t) = \int_{t-T_w}^{t} i_r(\tau)\exp(-j\omega_e\tau)\,d\tau \tag{3}$$

where $T_w$ is data window length, the finite Fourier transform of eqn. (1) becomes:

$$\overline{V}_r(j\omega_e, t) = R\,\overline{I}_r(j\omega_e, t) + j\omega_e L\,\overline{I}_r(j\omega_e, t) + L\,(i_r(t)\exp(-j\omega_e t) - i_r(t-T_w)\exp[-j\omega_e(t-T_w)]) \tag{4}$$

It can be seen that the last term in the RHS of eqn.(4) account for the sudden drop to zero of the time function at the beginning and at the end of the window duration. Decomposing $\overline{V}_r$, $\overline{I}_r$ into their real and imaginary parts gives,

$$\overline{V}_r(j\omega_e, t) = \overline{V}_{r1} - j\overline{V}_{r2} \tag{5}$$

$$\overline{I}_r(j\omega_e, t) = \overline{I}_{r1} - j\overline{I}_{r2} \tag{6}$$

where $\overline{V}_{r1}$, $\overline{V}_{r2}$, $\overline{I}_{r1}$, $\overline{I}_{r2}$ can be evaluated by the following equations

$$\overline{V}_{r1} = \int_{t-T_w}^{t} v_r(\tau)\cos(\omega_e\tau)\,d\tau \tag{7}$$

$$\overline{V}_{r2} = \int_{t-T_w}^{t} v_r(\tau)\sin(\omega_e\tau)\,d\tau \tag{8}$$

$$\overline{I}_{r1} = \int_{t-T_w}^{t} i_r(\tau)\cos(\omega_e\tau)\,d\tau \tag{9}$$

$$\overline{I}_{r1} = \int_{t-T_w}^{t} i_r(\tau)\sin(\omega_e\tau)\,d\tau \tag{10}$$

Eqn.(4) can then be arranged in the form,

$$\begin{bmatrix}\overline{V}_{r1}\\ \overline{V}_{r2}\end{bmatrix} = \begin{bmatrix}\overline{I}_{r1} & C_o\\ \overline{I}_{r2} & S_i\end{bmatrix}\begin{bmatrix}R\\ L\end{bmatrix} \tag{11}$$



where

$$C_o = i_r(t)\cos(\omega_e t) - i_r(t-T_w)\cos[\omega_e(t-T_w)] + \omega_e\overline{I}_{r2} \tag{12}$$

$$S_i = i_r(t)\sin(\omega_e t) - i_r(t-T_w)\sin[\omega_e(t-T_w)] - \omega_e\overline{I}_{r1} \tag{13}$$

When the matrix of the above equation is inverted, R and L can then be expressed as

$$\begin{bmatrix}R\\ L\end{bmatrix} = \frac{1}{\Delta}\begin{bmatrix}S_i & -C_o\\ -\overline{I}_{r2} & \overline{I}_{r1}\end{bmatrix}\begin{bmatrix}\overline{V}_{r1}\\ \overline{V}_{r2}\end{bmatrix} \tag{14}$$

where $\Delta = \overline{I}_{r1}S_i - \overline{I}_{r2}C_o$.

Hence a measurement of the line impedance as seen from the relaying point has been achieved.

## 3 Discrete digital signal processing

To achieve fast operation of the protective relay, real time calculation must be a minimum. Referring to eqn.(14), the first step is to calculate $\overline{V}_{r1}$, $\overline{V}_{r2}$, $\overline{I}_{r1}$, $\overline{I}_{r2}$. For the n-th elemental strip, the area A(n) is estimated by equation (15) to make use of the information conveyed by $\cos(\omega_e\tau)$ [Appendix 2].

$$A_n = \frac{1}{2}(v_r(t_{n-1}) + v_r(t_n))\int_{t_{n-1}}^{t_n}\cos(\omega_e\tau)\,d\tau \tag{15}$$

Therefore,

$$\overline{V}_{r1} = \frac{1}{2\omega_e}\sum_{n-1}^{N}([v_r(t_{n-1}) + v_r(t_n)][\sin(\omega_e t_n) - \sin(\omega_e t_{n-1})]) \tag{16}$$

where N is the number of samples in one data window.

To reduce the computing task, $V_{r1}$ is calculated by modifying the previous integral as follows:

$$\overline{V}_{r1}(k) = \overline{V}_{r1}(k-1) + [v_r(t_k) + v_r(t_{k-1})]*C(k) - [v_r(t_{k-N}) + v_r(t_{k-1-N})]*C(k-N) \tag{17}$$

where $\overline{V}_{r1}(k-1)$ = the result calculated in last sample period
and $C(k) = \sin(\omega_e t_n) - \sin(\omega_e t_{n-1})$.

In a similar way, $\overline{V}_{r2}(k)$, $\overline{I}_{r1}(k)$, $\overline{I}_{r2}(k)$, S(k), C(k), D(k) (D(k)=Δ(k)) can be calculated. The measured resistance and reactance at the sample instant k are calculated from eqn. (14) as follows:

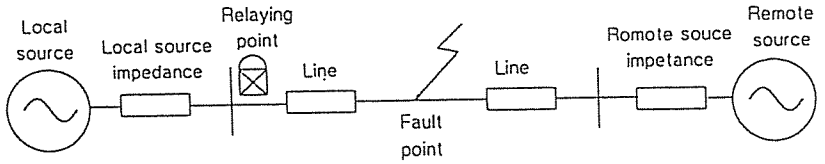
$$R(k) = [S_i(k)\,\overline{V}_{r1}(k) - C_o(k)\,\overline{V}_{r2}(k)] \,/\, D(k) \tag{18}$$

$$X(k) = 2\pi f L(k) = 2\pi f[\overline{I}_{r1}(k)\overline{V}_{r2}(k) - \overline{I}_{r2}(k)\overline{V}_{r1}(k)]/D(k) \tag{19}$$

In order to achieve an ultra fast operating speed, a sampling frequency of 4 kHz is used. A simple analogue lowpass filter is simulated to filter any component above 2 kHz in order to eliminate the aliasing effect. As the low pass analogue filter has a high cut-off frequency, the time delay caused by the filter is a minimum.

## 4. Digital relay simulation

The relay algorithm was simulated in a high level language. Fault transient voltage and current waveforms are generated by a method similar to that developed by A.T. Johns [9]. This method has an accurate representation of the frequency variance of line parameters and shows that even on lines which are electrically short, very severe transient conditions can exist. The typical line used for study here is a 400 kV double circuit overhead line, 128 km in length with a total line impedance of $36.8 \angle 86^\circ$ Ω. The system model and its parameters are showed in fig.1.




Fault level at relaying end = 35 GVA
Fault level at remote end = 35 GVA
Pre-fault relaying end busbar voltage = $1.0 \angle 0^\circ$
Pre-fault remote end busbar voltage= $1.0 \angle 30^\circ$
Total line impedance = $36.8 \angle 86^\circ$ Ω
Figure 1 System diagram for study case

A quadrilateral trip decision logic is used in this protection scheme (Fig.2). To protect 80 % of the line length, the relay reach is adjusted to:

$$X = 29.4\ \Omega;\quad X_0 = -4.0\ \Omega;\quad R = 29.4\ \Omega;\quad R_0 = -4.0\ \Omega.$$

To overcome the oscillation of calculated impedance in cases where the faulted voltage and current waveform are seriously distorted, a counter method is adopted for the relay operating logic. The protected region is divided into two zones[5]: the increased counter rate region and the reduced counter rate region. The relay counter will start to accumulate from zero whenever the impedance calculated falls within the operating region from the instant of fault inception. The settings used for study is shown in Fig.2.

Reduced counter rate region = 80 % to 100 % of relay reach
Increased counter rate = 2
Reduced counter rate = 1



Decrease counter rate = -1 (impedance outside the relay operating zone)

Final counter value = 8

## 5. Result of simulation

Simulations of the algorithm using the above system model under different fault condition (different fault type and different fault location) have been done. Some of the result is showed in Fig.3-6.

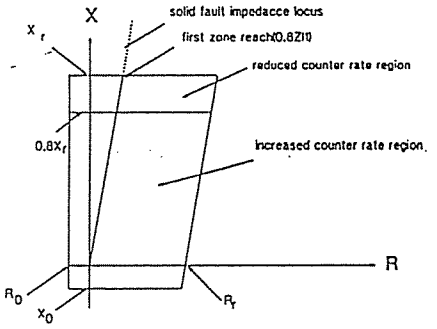


Figure 2 Relay tripping characteristic

It can be know that even under the influence of prefault load current, the algorithm still possessess a good discrimination and a high operating speed. The operating speed is within 5ms under normal conditions(Fig3, 4) and 7ms under an unfavorable condition(Fig5 ).

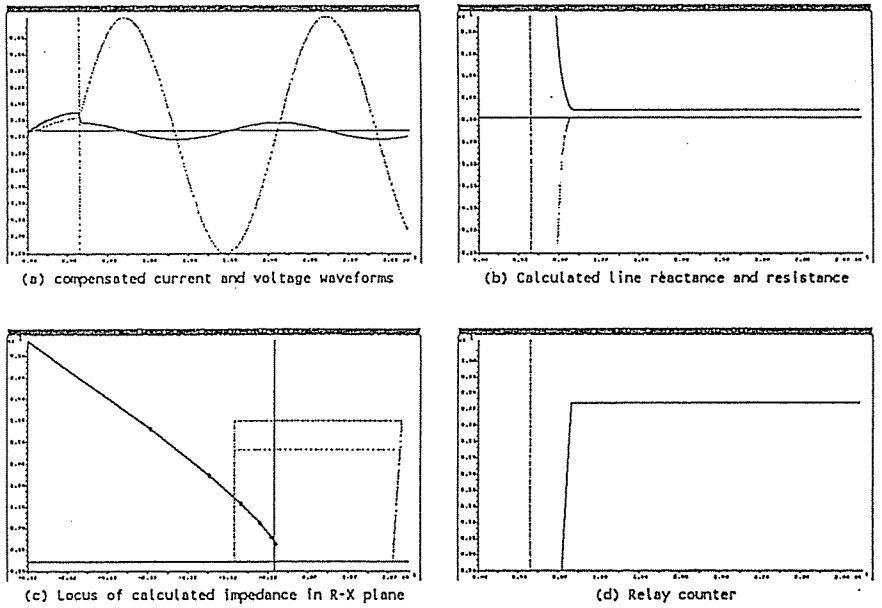



Figure 3 3-phase fault at 12.8km (10% of line length)

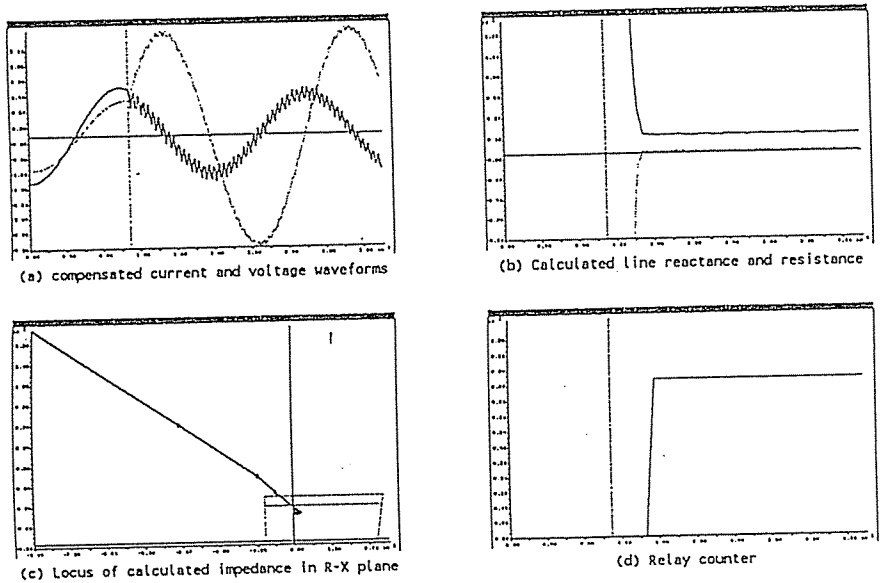



Figure 4 Phase-phase fault (B-C) at 64km (50% of line length)

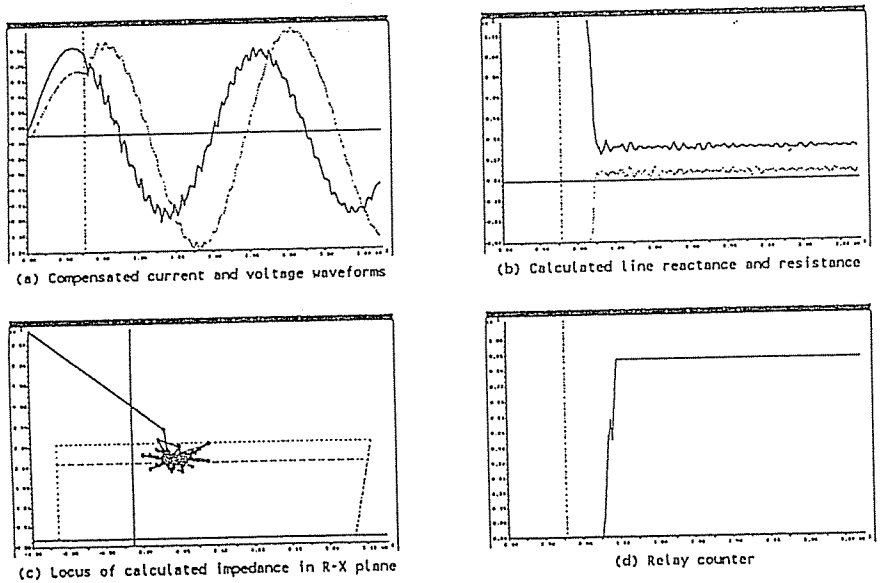



Figure 5 Phase-A to earth fault at 92km (72% of line length)



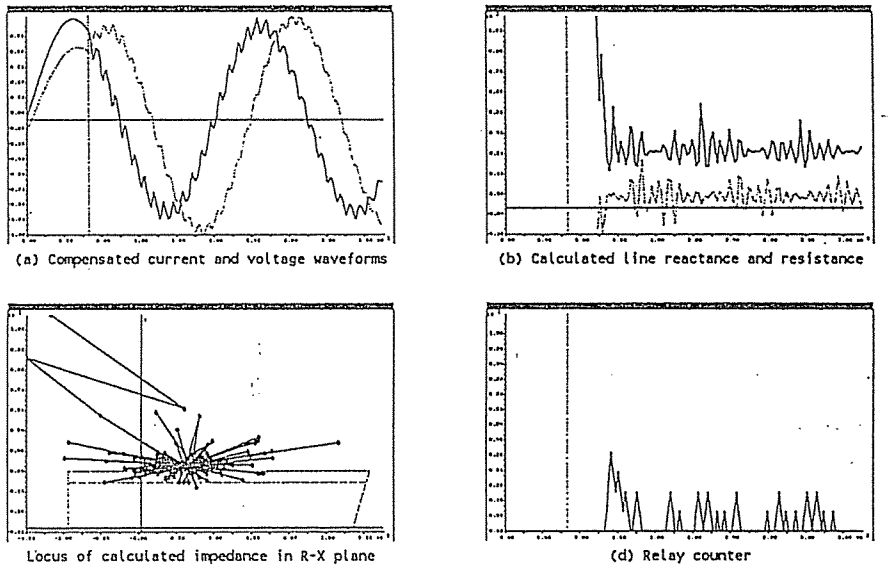



Figure 6 Phase-A to earth fault at 120km (94% line length)

## 6. Hardware design and real time simulation of digital relay

As a high sampling frequency(4kHz) is employed, only 250$\mu$s is available for A/D conversion, calculation of R(k) and X(k) and all trip logic judgment.

A parallel processing hardware scheme is designed. Fig.7 shows the block diagram.

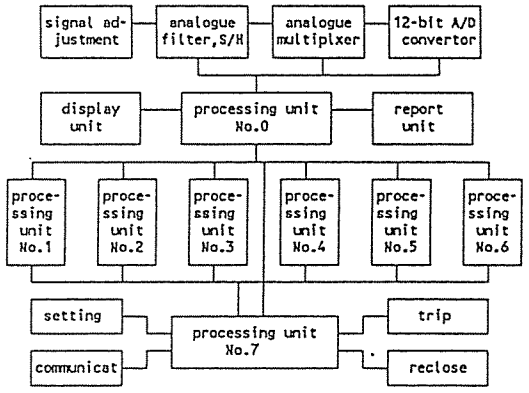



Figure 7 Hardware design of the digital relay

Signal adjustment unit adjusts and converts the power system voltages and current signals to a proper voltage level. Through analogue lowpass antialiasing filters, the multiple channel signals are sampled and hold simultaneously by S/H unit. A high speed A/D convertor with an analogue multiplexer converts the sampled signals sequentially. Processing unit No.0 control the signal convert units and transfer the digital data to processing unit No.1 to

No.6 which complete the relay function in parallel. Processing unit No.7 assumes the overall responsibility of logic judgment and time delay functions. The relay setting function is realized in this unit through setting panel. Connected with other processing units through interface, processing No.0 plays the role of monitoring the relay setting pattern, the situation of other processing unit and the power system signal waveform through display unit. The processing unit No.0 can be connected to a host computer system through intelligent I/O interface. The host computer can take the place of display and report unit.

In the hardware scheme, using parallel processing units to calculate different faults can reduce the real-time processing task for it is unnecessary to classify the fault type. The reliability of the relay can be improved significantly.

Real time simulation of the digital relay has been done on an IBM PC AT which has the same microprocessor as the target system. The program is written in assemble language with the objective of cutting down the on-line processing time. Fig.8 shows the flowchart of the digital. The input data produced by the

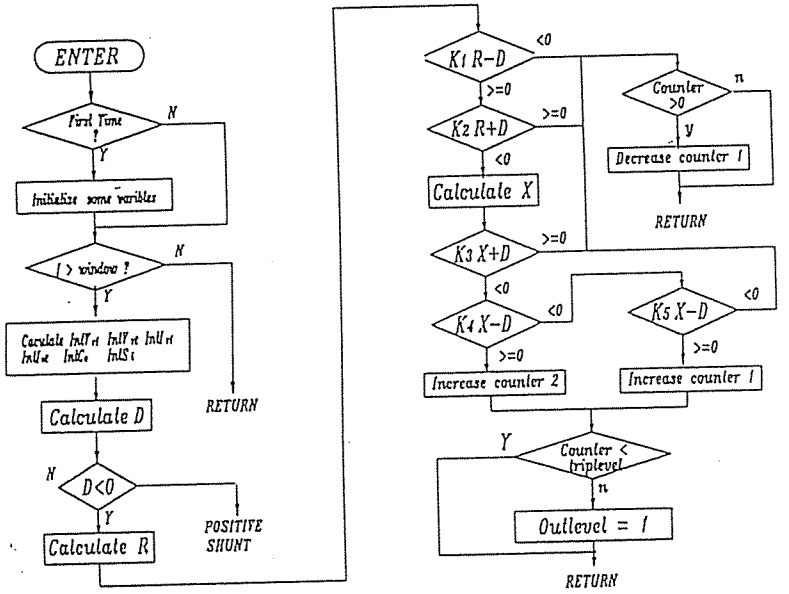



Figure 8 The flowchart of the digital relay



transient waveform simulation are converted to integer type in the main program. This will create the same processing environment as the planned target hardware system. When the execution of the digital relay is completed, the counter within the PC is read to give the exact processing time. The main program then displays the relay output. Fig.9 shows the flowchart of the main program.

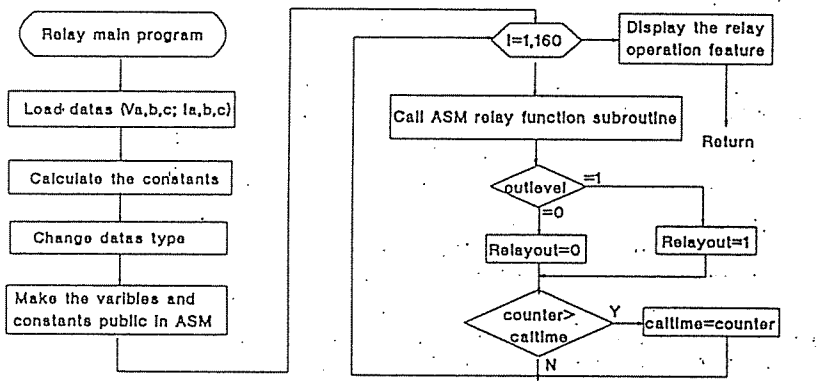



Figure 9 The flowchart of main program

The result of the real time simulation shows that all the required processing can be completed within 250 $\mu$s based on a 4 kHz sampling rate. A typical processing time is 150 $\mu$s on a 80286 CPU running at 12 MHz.

## 6. Conclusion

The finite transform algorithm possesses a strong filter function even with a very short data window. The calculated impedance can converge to its actual value rapidly and the on-line calculation is small. The technique for discrete digital signal processing largely reduces the real processing work.

The simulation of the algorithm proves that the relay can operate in an ultra-high-speed with high reliability and accuracy. The real time simulation shows that the calculation of resistance and reactance and all the trip logic judgment can be completed within one sampling interval.

The full digital approach greatly simplifies the hardware design and standard hardware system can be used. All these features make it very suitable to application in distance protection scheme for e.h.v transmission line.

## 7. Acknowledgments

The authors would like to thank the Department of Electrical Engineering Hong Kong Polytechnic for the laboratory and computing facilities, and the Research Sub-Committee of Hong Kong Polytechnic for the provision of grants to make this project possible. Thanks also go to the Department of Electrical Power Engineering & Automation, Tianjin University for technical support.

## 8. References

1. G. D. Rockefeller, "Fault Protection with a Digital Computer", IEEE Trans on PAS, Vol. PAS-88, pp.438-464, 1969.

2. S. Bergman, B. Lindquist, "Digital Technology in Protection Relaying", ASEA Journal, Vol. 59, No.1, pp. 20-23, 1986.

3. K. L. Hicks, W. H. Butt, "Feasibility and Economics of Ultra-High_Speed Fault Clearing", IEEE Trans. on PAS, Vol. PAS-99, No.6, pp.2138-2143, 1980.

4. A. G. Phadke, T. Hlibka, and etc, "A Microcomputer Based Ultra-High-Speed Distance Relay: Field Tests", ibid, Vol. PAS-100, No.4, pp.2026-2033, 1981.

5. A. T. Johns, M. A. Martin, "New Ultra-High-Speed Distance Protection Using Finite-Transform Techniques", IEE Proc., Vol. 130, Pt. C, No.3, pp.127-138, May 1893.

6. A. T. Johns, M. A. Martin, and etc., "A New Approach to E. H. V. Direction Comparison Protection Using Digital Signal Processing Techniques", IEEE Trans. on PWRD, Vol. PWRD-1, No.2, pp.24-34, April 1986.

7. K. S. Prakash, O. P. Malik, G. S. Hope, "Amplitude Comparator Based Algorithm for Directional Comparison Protection of Transmission Lines", ibid, Vol. PWRD-4, No.4, pp.2032-2041, October 1989.

8. A. Wiszniewski, "Digital High-Speed Calculation of the Distorted Signal Fundamental Component", IEE Proc., Vol.137, Pt.C, No.1, pp.24, January 1990.

9. A. T. Johns, R. K. Aggarwal, "Digital Simulation of Faulted E. H. V. Transmission Lines with Particular Reference to Very-High-Speed Protection", ibid, Vol.123, No.4, pp.353-359, April 1976.





# A TECHNIQUE FOR SIMULATING DIGITAL RELAYS FOR DISTANCE PROTECTION

D.L. Waikar
MIEEE, MIE(I), Lecturer
Electrical Engg Department
Singapore Polytechnic
Singapore 0513

M.S. Sachdev
FIEEE, FIEE, FIE(I), Prof. and Head
Electrical Engg. Department
University of Saskatechwan
Saskatoon, Canada S7N 0W0

## ABSTRACT

Relaying with digital computer has been an attractive field of research for many researchers since 1970's. Developments in digital processors have enabled researchers to design complex relaying systems with a view to improvise the protection of power system equipment. Simulation technique is one of the useful tools in implementing and evaluating the performance of the designed relays. This paper describes the usefulness of such a technique for designing and simulating a digital relay for the protection of transmission lines. As distance relays are used for protecting transmission lines, an approach described in the paper is focused on simulating a digital distance relay. This paper proposes the simulation algorithm that can be used for simulating a distance relay on the digital computer. The application of the proposed algorithm is demonstrated by simulating the major functional subsystems of a digital distance relay on VAX 8650 digital computer. The performance of the simulated relay was evaluated using fault data obtained from transmission line model and the Electro-Magnetic Transient Program (EMTP). Some results of the case studies are reported in the paper.

## 1. INTRODUCTION

Relaying with digital computer has been an attractive field of research for many researchers since 1970's. The initial approach of using a single digital computer for the protection functions [1] has been discarded due to the recent developments in the digital processors [2]. These developments have enabled researchers to design complex relaying systems with a view to improvise the protection of power system equipment. It is envisaged that future digital relays will be viable alternatives to the electro-mechanical and solid-state relays. As distance relays are used for protecting transmission lines, an approach described in the paper is focused on simulating a digital distance relay.

Simulation is one of the useful techniques in evaluating the relay designs. This paper describes the usefulness of such a technique in designing and simulating a digital relay for the protection of transmission lines. The functions of the proposed simulation algorithm are also briefly explained.

**1.1 Digital Distance Relay:** A typical digital distance relay has several subsystems with defined functions. The actual subsystems may have configuration that is different